PTO/SB/08A (10-01)

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Substitute	Substitute for form 1449A/PTO			Complete if Known		
				Application Number	R53(b) DIV, of S.N. 09/829,969	
INFORMATION DISCLOSURE				Filing Date	March 31, 2004	
	STATEMENT BY AP	PLICA	ANT	First Named Inventor	K. OHNISHI	
				Art Unit	2818	
	(use as many shoets as n	ocessar	γ)	Examiner Name	M. TRAN	
Sheet	1	of	2	Attorney Docket Number	500.40010VX1	

U.S. PATENT DOCUMENTS						
Examiner Initials'	Cite No.1	Document Number Number-Kind Code ² (if known)	Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear	
UK		US-6.291.868	09/2001	Weimer et al		
		US-6.265.297	07/2001	Powell		
		US-6,306,743	10/23/2001	Lee		
V		US-2002/0008294	01/24/2002	Hayashi et al		
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		FOREIG	N PATENT DOC	UMENTS		
Examiner Initials'	Cite No.1	Foreign Patent Document	Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear	T ^d
		Country Code ³ -Number ⁴ -Kind Code ⁶ (if known)				
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^{*}EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.

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Substitute	Substitute for form 1449B/PTO			Complete if Known		
				Application Number	R53(b) DIV. of S.N. 09/829,969	
INFORMATION DISCLOSURE STATEMENT BY APPLICANT				Filing Date	March 31, 2004	
				First Named Inventor	OHNISHI, K.	
				Group Art Unit	2818	
(use as many sheets as necessary)			nd	Examiner Name	M. TRAN	
Sheet	2	of	2	Attorney Docket Number	500.40010VX1	

		OTHER PRIOR ART—NON PATENT LITERATURE DOCUMENTS	
Examiner Initials*	Cite No.	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the Item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s),	₹2
uft	_	OHNISHI, K., et al., "Improving Gate Oxide Integrity of a W/WNx/dual-poly Si Stacked-Gate by Using Wet- Hydrogen Oxidation in 0.14-µm CMOS Devices," IEDM Technical Digest, Pgs. 397-400, IEDM 98, USA.	
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